Notice of References Cited	Application/Control No. 09/749,590	Applicant(s)/Patent Under Reexamination OHTAKE ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6080645	06-2000	Pan	438/585
	B	US-Pub 2001/0000629	05-2001	Tsukamoto	438/585
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	K. Kasai et al., W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs. IEDM 1994, pp. 497-500.
	V	Y. Akasaka et al., Low-Resitstivity Poly-Metal Gate Electrode Durable for High-Temperature Processing. IEEE 1996, pp. 1864-1869.
	W	B. H. Lee et al., In-Situ Barrier Formation for High Reliable W/Barrier/Poly-Si Gate Using Denudation of WNx on Polycrystalline Si. IEDM 1998, pp. 385-388.
	X	Y. Hiura et al., Integration Technology of Polymetal (W/WSiN/Poly-Si) Dual Gate CMOS for 1Gbit DRAMs and Beyond. IEDM 1998, pp. 389-392.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.